UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,758	12/20/2000	Takao Watanabe	HIT 2 482-06	7380

24956 7590 09/26/2003

MATTINGLY, STANGER & MALUR, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER
HIRL, JOSEPH P

ART UNIT	PAPER NUMBER
2121	12

DATE MAILED: 09/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,758	WATANABE ET AL.	
	Examiner	Art Unit	
	Joseph P. Hirl	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *July 10, 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is in response to an AMENDMENT entered July 10, 2003 for the patent application 09/739,758 filed on December 20, 2000.

2. The First Office Action of April 17, 2003 is fully incorporated into this Final Office Action by reference.

3. The claims and only the claims form the metes and bounds of the invention. "Office personnel are to give the claims their broadest reasonable interpretation in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d, 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)" (MPEP page 2100-8, col 2 lines 45-48; page 2100-9, col 1, lines 1-4). The Examiner has full latitude to interpret each claim in the broadest reasonable sense. Examiner will reference prior art using terminology familiar to one of ordinary skill in the art. Such an approach is broad in concept and can be either explicit or implicit in meaning.

Status of Claims

4. Claims 25-32 are amended. Claims 33-37 are new. Claims 25-37 are pending.

Claim Rejection

5. Claims 25-27, 29, 33, 34, 36, rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 25-27, 29, 33, 34, 36

See para 3 above. The specification is silent on "first mode" and "second mode."

Response to Arguments

6. The objection to the Information Disclosure Statement remains. The earlier application was not identified in the IDS and hence 37 CFR 1.98(d) does not apply.

7. The objection to the drawings remains. U.S. Patent 6,205,556 was granted on March 20, 2001 and the drawings of U.S. Patent 6,205,556 are identical to those of the instant application.

Figures 1-25 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

8. The objection to the Abstract is withdrawn.

9. The rejection of Claims 29 and 30 under 35 USC 112, first paragraph, concerning first and second memory arrays, and first and second signal paths is withdrawn.

10. Applicant's arguments filed on July 10, 2003 related to Claims 25-37 have been fully considered but are not persuasive.

In reference to Applicant's argument:

The semiconductor integrated circuit device, as recited in claim 25, has first and second modes. In the first mode, read and write operation to the memory array are performed. In the second mode, information is read from the memory array to the processing circuit. Also, during the first mode, a MOS transistor, which has a source/drain path between an arithmetic unit in the processing circuit and a power line, is in an OFF state. This allows for lower power consumption when the processing circuit is not carrying out operation.

Mashiko does not disclose or suggest two modes having features as in claim 25. Since the switching elements S1, S2, S3, S4 are each controlled by information stored in the random memory cells 150, 151, and output of an amplifier Ci, there is no disclosure of two modes as in claim 25. Also, Mashiko does not disclose or suggest a MOS transistor between an arithmetic unit and a power line, which is in a OFF state during a mode when read and write operations are performed.

Examiner's response:

See para 3 above. The specification is silent on "first mode" and "second mode." While the specification cites the use of an MOS transistor in many instances, the Examiner was unable to identify in the specification "during the first mode, a MOS transistor, which has a source/drain path between an arithmetic unit in the processing circuit and a power line, is in the OFF state." New matter is not allowed and the arguments related to Mashiko are therefore moot.

In reference to Applicant's argument:

The semiconductor integrated circuit device, as recited in claim 29, includes a first bus coupled between the first memory array and the logic circuit; a second bus coupled between the logic circuit and the input/output circuit; and a third bus coupled between the first memory array and the input/output circuit. The semiconductor-integrated device also has a first and second mode. In the first mode, by using the

third bus, information from outside the semiconductor chip is written to the first memory array or information is read out of the semiconductor chip from the first memory array. In the second mode, by using the first bus, information is read from the first memory array to the logic circuit. By using the second bus, the logic circuit outputs results of the operation to the latch circuit. Also, by using the third bus, data in accordance with the results is written to the first memory array.

Mashiko does not disclose or suggest a second bus coupled between the logic circuit and input/output circuit. While Mashiko does disclose a bus coupled between switching elements and random memory cells 150, 151, and a bus coupled between random memory cells 150, 151 and interface(I/O), Mashiko does not disclose any separate bus for coupling the logic circuit and input/output circuit. Mashiko also does not disclose or suggest a first and second mode, as cited in claim 29.

Examiner's response:

See para 3 above. Applicant's analysis identifies two buses as stated above. To one of ordinary skill in the art, a logic circuit is an electronic circuit that processes information by performing a logical operation on it. Such a circuit produces an output based on the rules of logic it is designed to follow for the electrical signals it receives as input. In reference to Fig. 5 of Mashiko at col 3 lines 45-46, "The switching element S2 is on-off controlled by the information in the random access memory cell 150." This is a logic operation. Thus the coupling of the random cells and the interface is one instance of a logical operation. Above comments regarding first and second modes apply.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Claims 25-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Mashiko (U. S. Patent 4,988,891 referred to as **Mashiko**). See prior office actions for other rejections.

See prior office actions for claims for rejection rationale related to claims 25-27, 29, 33, 34, 36 which are rejected above in this instant office action on the basis of new matter.

Claim 28

Mashiko anticipates each of the plurality of memory cells includes a MOS transistor and a capacitor, and said processing circuit is formed by MOS transistors, and wherein said semiconductor integrated circuit device is formed on a semiconductor ship (**Mashiko**, col 15, lines 53-67; Examiner's Note (EN): Fig. 1 is a representation of a neuron. Fig. 4 is a schematic of a neural network. Column 4, lines 17-24 identify the transition from the neuron to the neural network. Neural networks have memory that resides in the network...weights and interconnectivity. The circuit implementation of figure 4 uses electronic solid state components to achieve the VLSI configuration of column 2, lines 37-41. Mashiko implements his invention using Metal Oxide Semiconductors (MOS) and other generic electronic components such as capacitors such as those components identified in column 15, lines 42-52; to one of ordinary skill in the art, a semiconductor integrated circuit is formed on a semiconductor chip; **Mashiko**, col 3 lines 4-5).

Claim 30

Mashiko anticipates a second memory array including a plurality of DRAM

memory cells coupled to said logic circuit and said input/output circuit , wherein said logic circuit is placed between said first memory array and said second memory array and receives outputs said first memory array and said second memory array (**Mashiko**, col 2, lines 37-67; col 3, lines 52-61).

Claim 31

Mashiko anticipates a converting circuit which converts said results to said data so that a number of bits used for said data is equal to a number of bits used for information read out to said logic circuit, wherein each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor (**Mashiko**, col 2, lines 37-67; col 3, lines 52-61; EN: above comments apply; the converting circuit as claimed is an non event; specifically if the case is represented by a binary design and there are N bits on the input and N bits on the output, to one of ordinary skill in the art, there has been no conversion...each input bit equals each output bit).

Claim 32

Mashiko anticipates each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor (**Mashiko**, col 2, lines 37-67; col 3, lines 52-61; EN: above comments apply).

Claim 35

Mashiko anticipates a comparing circuit comparing said results with an expected value (**Mashiko**, col 6, lines 1-2).

Claim 37

Mashiko anticipates first memory array and second memory array each includes sense amplifiers and a precharged circuit (**Mashiko**, col 3, lines 28-51; EN: sets of RAM 1 constitute first memory array; sets of Ram 2 constitute RAM 2; all amplifiers sense their input; all circuits are precharged upon initialization to initial conditions by design).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

Any inquiry concerning this information or related to the subject disclosure should be directed to the Examiner, Joseph P. Hirl, whose telephone number is (703) 305-1668. The Examiner can be reached on Monday – Thursday from 6:00 a.m. to 4:30 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Anil Khatri can be reached at (703) 305-0282.

Any response to this office action should be mailed to:

Commissioner of Patents and Trademarks,

Washington, D. C. 20231;

or faxed to:

(703) 746-7239 (for formal communications intended for entry);

or faxed to:

(703) 746-7290 (for informal or draft communications with notation of "Proposed" or "Draft" for the desk of the Examiner).

Hand-delivered responses should be brought to:

Receptionist, Crystal Park II

2121 Crystal Drive,

Arlington, Virginia.

Joseph P. Hirl

September 23, 2003

ANIL KHATRI
SUPERVISORY PATENT EXAMINER